AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6. (Canceled)

Claim 7. (Currently Amended) A digitally controlled impedance driver circuit in ~~accordance with Claim 6,~~ comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first ideal resistance;

a second finger comprising a second field effect transistor unit having a second ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the second ideal effective length-to-width ratio is smaller than the first ideal effective length-to-width ratio, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second ideal resistance that is smaller than the first ideal resistance,

wherein the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio is between forty percent and sixty percent; and

a third finger comprising a third field effect transistor unit having a third ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third ideal effective length-to-width ratio is ninety to one hundred and ten percent of the second ideal effective length-to-width ratio, wherein the third finger further ~~including~~ includes a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node, the third resistor having a third ideal resistance that is ninety to one hundred and ten percent of the second ideal resistance.

Claim 8. (Currently Amended) A digitally controlled impedance driver circuit in accordance with Claim **[[6]]** 7, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

Claim 9. (Cancelled).

Claim 10. (Currently Amended) A digitally controlled impedance driver circuit in accordance with Claim **[[9]]** 7, wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one.

Claim 11. (Currently Amended) A digitally controlled impedance driver circuit in ~~accordance with Claim 1~~ comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first ideal resistance; and

a second finger comprising a second field effect transistor unit having a second ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the second ideal effective length-to-width ratio is smaller than the first ideal effective length-to-width ratio, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second ideal resistance that is smaller than the first ideal resistance, wherein the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio is below forty percent.

Claim 12. (Currently Amended) A digitally controlled impedance driver circuit in accordance with Claim 11, further comprising the following:

a third finger comprising a third field effect transistor unit having a third ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third ideal effective length-to-width ratio is ~~approximately equal to~~ ninety to one hundred and ten percent of the second ideal effective length-to-width ratio~~, the third resistor having a third ideal resistance that is approximately equal to the second ideal resistance~~.

Claim 13. (Currently Amended) A digitally controlled impedance driver circuit in accordance with Claim 12, wherein the third finger further ~~including~~ includes a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node.

Claim 14. (Original) A digitally controlled impedance driver circuit in accordance with Claim 12, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

Claim 15. (Cancelled)

Claim 16. (Currently Amended) A digitally controlled impedance driver circuit in accordance with Claim 12 [[15]], wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one.

Claim 17. (Canceled).

Claim 18. (Currently Amended) A digitally controlled impedance driver circuit ~~in accordance with Claim 1, further~~ comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first ideal resistance; and

a second finger comprising a second field effect transistor unit having a second ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the second ideal effective length-to-width ratio is smaller than the first ideal effective length-to-width ratio, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second ideal resistance that is smaller than the first ideal resistance; and

a third finger comprising a third field effect transistor unit having a third ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third ideal effective length-to-width ratio is ~~approximately equal to~~ ninety to one hundred and ten percent of the second ideal effective length-to-width ratio~~, the third resistor having a third ideal resistance that is approximately equal to the second ideal resistance~~.

Claim 19. (Currently Amended) A digitally controlled impedance driver circuit in accordance with Claim 18, wherein the third finger further ~~including~~ includes a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node.

Claim 20. (Original) A digitally controlled impedance driver circuit in accordance with Claim 18, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

Claim 21. (Cancelled).

Claim 22. (Currently Amended) A digitally controlled impedance driver circuit in accordance with Claim 18 [[21]], wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one.

Claims 23 and 24. (Canceled).

Claim 25. (Currently Amended) A digitally controlled impedance driver circuit in ~~accordance with Claim 1~~ comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first ideal resistance; and

a second finger comprising a second field effect transistor unit having a second ideal effective length-to-width ratio and having a source terminal coupled to the first voltage supply,

wherein the second ideal effective length-to-width ratio is smaller than the first ideal effective length-to-width ratio, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second ideal resistance that is smaller than the first ideal resistance, wherein the digitally controlled impedance driver circuit comprises at least third, fourth, and fifth fingers, each having approximately the same impedance when turned on as the second finger, the digitally controlled impedance driver circuit further comprising the following:

a controller circuit configured during operation to periodically determine a configuration of the digitally controlled impedance driver circuit that would result in the digitally controlled impedance driver circuit approximating a target impedance;

a comparator configured to determine if the impedance of the digitally controlled impedance driver circuit should be increased or decreased; and

a noise attenuation circuit configured to turn off only one of the second, third, fourth or fifth fingers if the controller circuit determines that more impedance is needed even if turning off only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

Claim 26. (Original) A digitally controlled impedance driver circuit in accordance with Claim 25, wherein the noise attenuation circuit is further configured to turn on only one of the second, third, fourth or fifth fingers if the controller circuit determines that less impedance is needed even if turning on only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

Claim 27. (Original) A digitally controlled impedance driver circuit in accordance with Claim 25, wherein the controller circuit is configured to periodically make the determination of the configuration more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to a load, and wherein the noise attenuation circuit is configured to adjust the configuration of the digitally controlled impedance driver circuit more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to the load.

Claims 28 and 29. (Canceled).

Claim 30. (Currently Amended) A digitally controlled impedance driver circuit ~~in accordance with Claim 28, further~~ comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first resistance;

a second finger comprising a second field effect transistor unit having a second effective length-to-width ratio and having a source terminal coupled to the first voltage supply, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second

resistance, wherein the ratio of the second effective length-to-width ratio to the first effective length-to-width ratio is less than sixty percent; and

a third finger comprising a third field effect transistor unit having a third effective length-to-width ratio and having a source terminal coupled to the first voltage supply, wherein the third effective length-to-width ratio is ~~approximately equal to~~ ninety to one hundred and ten percent of the second effective length-to-width ratio~~, the third resistor having a third resistance that is approximately equal to the second resistance~~.

Claim 31. (Original) A digitally controlled impedance driver circuit in accordance with Claim 30, wherein the third finger further includes a third resistor coupled in series between a drain terminal of the third field effect transistor unit and the input/output node.

Claim 32. (Original) A digitally controlled impedance driver circuit in accordance with Claim 30, wherein the second transistors couples a drain terminal of the third field effect transistor unit to the input/output node.

Claims 33 and 34. (Cancelled).

Claim 35. (Currently Amended) A digitally controlled impedance driver circuit ~~in accordance with Claim 28~~ comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

a first finger comprising a first field effect transistor unit having a first effective length-to-width ratio and having a source terminal coupled to the first voltage supply, and further comprising a first resistor coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first resistance;

a second finger comprising a second field effect transistor unit having a second effective length-to-width ratio and having a source terminal coupled to the first voltage supply, the second finger further including a second resistor coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second resistance, wherein the ratio of the second effective length-to-width ratio to the first effective length-to-width ratio is less than sixty percent, wherein the digitally controlled impedance driver circuit comprises at least third, fourth, and fifth fingers, each having approximately the same impedance when turned on as the second finger, the digitally controlled impedance driver circuit further comprising the following:

a controller circuit configured during operation to periodically determine a configuration of the digitally controlled impedance driver circuit that would result in the digitally controlled impedance driver circuit approximating a target impedance;

a comparator configured to determine if the impedance of the digitally controlled impedance driver circuit should be increased or decreased; and

a noise attenuation circuit configured to turn off only one of the second, third, fourth or fifth fingers if the controller circuit determines that more impedance is needed even if turning off only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

Claim 36. (Original) A digitally controlled impedance driver circuit in accordance with Claim 35, wherein the noise attenuation circuit is further configured to turn on only one of the second, third, fourth or fifth fingers if the controller circuit determines that less impedance is needed even if turning on only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

Claim 37. (Original) A digitally controlled impedance driver circuit in accordance with Claim 35, wherein the controller circuit is configured to periodically make the determination of the configuration more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to a load, and wherein the noise attenuation circuit is configured to adjust the configuration of the digitally controlled impedance driver circuit more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to the load.

Claim 38. (Original) A digitally controlled impedance driver circuit comprising the following:

a first voltage supply that is configured to carry a first voltage during operation;

an input/output node upon which the digital controlled impedance driver circuit is to apply a signal during operation;

an array of fingers, each finger comprising a field effect transistor unit that is coupled between the first voltage supply and the input/output node, the field effect transistor units configured to operate in the linear region when the corresponding finger is on, and to be turned off when the finger is off;

a controller circuit configured during operation to periodically determine a configuration of the digitally controlled impedance driver circuit that would result in the digitally controlled impedance driver circuit approximating a target impedance;

a comparator configured to determine if the impedance of the digitally controlled impedance driver circuit should be increased or decreased; and

a noise attenuation circuit configured to turn off only one of the fingers if the controller circuit determines that more impedance is needed even if turning off only one finger would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

Claim 39. (Original) A digitally controlled impedance driver circuit in accordance with Claim 38, wherein the noise attenuation circuit is further configured to turn on only one of the second fingers if the controller circuit determines that less impedance is needed even if turning on only one would not result in the configuration of the digitally controlled impedance driver circuit determined by the controller circuit.

Claim 40. (Original) A digitally controlled impedance driver circuit in accordance with Claim 38, wherein the controller circuit is configured to periodically make the determination of the configuration more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to a load, and wherein the noise attenuation circuit is configured to adjust the configuration of the digitally controlled impedance driver circuit more frequently during power-up than when the digitally controlled impedance driver circuit is actually driving data to the load.